# Explain the architecture of VLIW processor and its pipeline operations.

# Explain the inclusion property and locality of reference along with its types in multilevel memory hierarchy. (or) Explain inclusion, coherence and locality properties.

# Explain page replacement policies with the help of an example.

# Give the characteristics of symbolic processors.

# What are the characteristic of CISC and RISC architecture?

# What are the virtual memory models for multiprocessor system?

# Explain address translation mechanism using TLB and page table.

# Explain typical superscalar RISC processor architecture.

# With a diagram, explain the models of a basic scalar computer system.

# ~~With a diagram, explain a typical superscalar RISC processor architecture consisting of an integer unit and a floating-point unit.~~

# With a diagram, explain the hierarchical memory technology.

**Module-3**

# What is arbitration? Explain different types of arbitration.

# Explain sequential and weak consistency models.

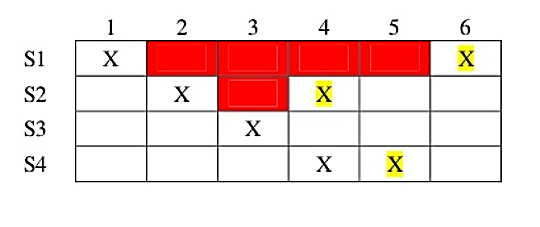
# What are the different techniques for branch prediction? Explain.

# Explain multiply pipeline design to multiply two 8-bit integers.

# Explain with diagram. the backplane bus specification.

# With the diagrams, explain the central arbitration and distribution arbitration.

# For the reservation table of a non-linear pipeline shown below:



i) What are the forbidden latencies? Write initial collision vector

ii) Draw the state transition diagram

iii) List all simple cycles and greedy cycles

iv) Determine MAL

# Explain prefetch buffer and internal data forwarding mechanisms used in instruction pipelining.

# Explain any two mapping techniques.

# Explain the following terms associated with cache and memory architecture:

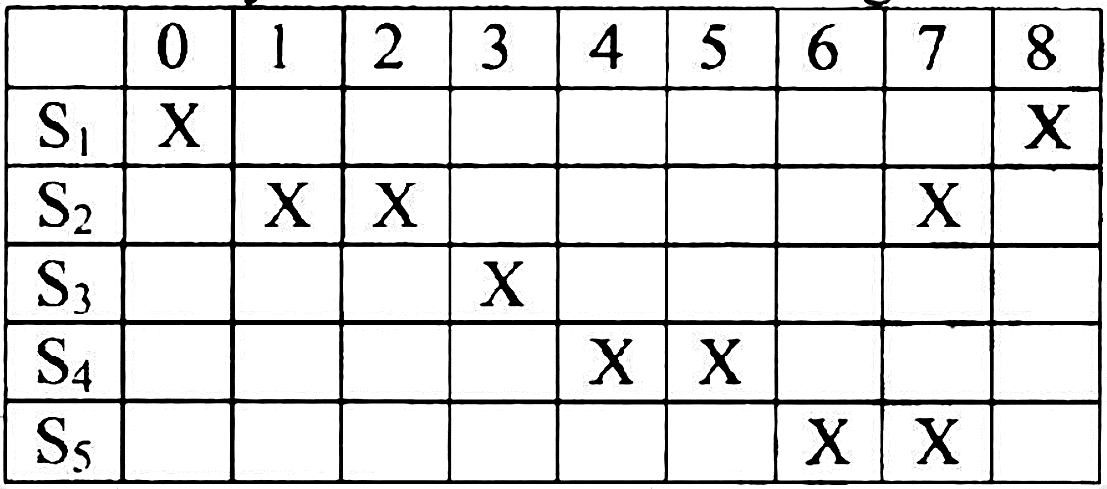
(i) Low order memory interleaving

(ii) Atomic vis non-atomic memory

(iii) Physical address cache vs virtual address cache

(iv) Memory bandwidth and fault tolerance.

# Consider the following pipelined processor within 3 stages this pipeline has total evaluation time of 8 clock cycles. All successor stages must be used after each clock cycle.



(i) List the set of forbidden latencies between task initiations

(ii)Draw the state diagram which shows all possible latency cycles

(iii) List all greedy cycles

(iv) Value of MAL.

# Explain routing in omega network.

# What are different vector – access memory schemes? Explain any two of them.

# What are the implementation models of SIMD? Explain them.

# Explain four context-switching policies.

# Explain crossbar networks and cross-point switch design in multiprocessor system.

# With necessary sketches, explain the cache-coherence problems in data sharing and in process migration.

# With a diagram, explain the architecture of the connection machine CM-2.

# Explain the context-switching policies.

# Explain hierarchical bus system with neat diagram.

# Explain crossbar networks along with its advantages and limitations.

# Explain snoopy protocols with its approaches.

# Briefly explain message routing schemes.

# What are the issues in using shared-variable model?

# Explain different phases of parallelizing compiler with a diagram.

# Explain testing algorithm for dependence testing. (page no. 528 Text- book)

# What are the principles of synchronization mechanisms? Explain them. (page 585 TB)

# Explain the concurrent OOP and an actor model in object - oriented model.

# Explain the fairness policies and sole-access -protocols in the principles of synchronization. (page 585 TB)

# What are the major hurdles of pipelining? Illustrate the branch hazards in detail.

# Explain the dynamic scheduling or a pipeline using Tomasulo 's algorithm.

# Define parallel programming model. Explain any two models.

# Mention branch prediction methods and explain.

# ~~With the help of a neat diagram explain compilation phases in code generator.~~

# Explain different language features for parallelism.